REMARKS

Claims 1-33 were pending, of which claims 1, 2-5 and 20 have been amended and claim 34 has been added. Reconsideration and allowance is respectfully requested in light of the foregoing amendments and the following remarks.

Claims 3, 4 and 5 have been amended to correct several errors identified by the Examiner. No new matter has been added.

Claims 1-33 stand rejected under 35 U.S.C. §§ 102(b) and 103(a) in light of US 6,383,861 (Gonzalez) either alone or in light of one or more other cited references. With respect to the claims as herein amended, this rejection is respectfully traversed.

The PTO provides in MPEP § 2131 that

> *"[t]o anticipate a claim, the reference must teach every element of the claim...."*

Claim 1 requires, *inter alia*, "removing said first insulator layer from the I/O region of said semiconductor substrate, resulting in a first gate insulator layer having a first insulator thickness, located on the core region of said semiconductor substrate." In contrast, Gonzalez teaches a method of making an oxide-nitride-oxide (ONO) layer 34 in the peripheral area 22 by removing the silicon nitride layer 26 from the memory area 20, leaving the peripheral area unchanged. (Figs. 4-5, col. 5, lines 11-12, col. 6, lines 41-43).

Claims 5 and 20, require that the thickness of the first insulator is less than the thickness of the second insulator. In contrast, Gonzalez teaches a method wherein the thickness of the ONO layer 34 is greater than the thickness of the oxide layer 32. (Fig. 9). This is because following the resist strip, both the periphery 22 and the memory array area 20 are subjected to the same thermal oxidation procedure. (col. 6, lines 7-10).

With respect to the rejection of claims 2, 3, and 21, the combination of references cited by the Examiner is improper hindsight. The MPEP § 2143.01 provides:

> *The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.*

Here, neither Gonzalez nor Lu et al. teaches, or even suggests, the desirability of the combination since Gonzalez is directed to forming an ONO layer and Lu is directed to recycling wafers. The fact that they are both in the general field of endeavor of semiconductor processing is not sufficient motivation. Creating an ONO layer and recycling wafers are sufficiently unrelated. It is the unique sequence of steps that, taken as a whole, is neither taught nor suggested by the prior art of reference and to rule otherwise would allow the Examiner to piece together any semiconductor processes using the claim as a roadmap.

The remaining dependent claims further limit their respective base claims and are also deemed to be in condition for allowance.

The Examiner is invited to contact the undersigned at the numbers provided below if further consideration is required. Also, Deposit Account No. 08-1394 may be used for any over or under payments.

Respectfully submitted,

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